

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Canceled)

2. (Currently Amended) A time division multiplex data recover system comprising:

3 a reference clock generator generating a reference clock signal;

4 a phase frequency comparator having a first input connected to  
5 said reference clock generator, a second input and an output  
6 generating a voltage proportional to a difference in phase and  
7 frequency between a signal received at said first input and a  
8 signal received at said second input;

9  
10 a voltage controlled oscillator having a voltage input  
11 connected to said output of said phase frequency comparator and  
12 plural a plurality of outputs each generating a corresponding clock  
13 signal at differing phases, each having a frequency proportional to  
14 a voltage received at said voltage input, said plural plurality of  
15 clock signals including a sampling clock signal and a leading clock  
16 signal having a phase leading said sampling clock signal by 90°;

17 a data recovery block having an input receiving a time  
18 division multiplexed data signal, a first clock input receiving  
19 said sampling clock signal and a second clock input receiving said  
20 leading clock signal, said data recovery block deserializing the  
21 received time division multiplexed data signal by sampling with  
22 said sampling clock signal, said data recovery block further  
23 sampling the received time division multiplexed data signal with  
24 said leading clock and generating an early/late signal indicating  
25 whether said sampling clock signal is early or late by comparing  
26 data value of the received time division multiplexed data signal

27 sampled with said sampling clock signal to data value of the  
28 received time division multiplexed data signal sampled with said  
29 leading clock;

30 a phase selection circuit connected to said data recovery  
31 block and receiving said early/late signal, said phase selection  
32 circuit generating an interpolation code indicative of an  
33 interpolation amount and a phase select code indicative of one  
34 phase sector of a plurality of phase sectors of said plural clock  
35 ~~signal of said voltage controlled oscillator~~ dependent upon said  
36 early/late signal, said phase sector disposed between an adjacent  
37 pair of said plurality of clock signals;

38 a phase interpolator having ~~plural~~ said plurality of clock  
39 inputs receiving ~~plural~~ said plurality of clock signals at  
40 differing phases of said voltage controlled oscillator, an  
41 interpolation input receiving said interpolation code and a phase  
42 select input receiving said phase select code, and said phase  
43 interpolator generating a single output signal of an interpolation  
44 of ~~two~~ said adjacent pair of said plurality of clock signals of  
45 ~~adjacent phases~~ corresponding to said interpolation code and said  
46 phase select code, said single output signal connected to said  
47 second input of said phase frequency comparator.

1       3. (Previously Presented) The time division multiplex data  
2 recover system of claim 2, wherein:

3       said voltage controlled oscillator includes a ring oscillator  
4 having a plurality of differential input, differential output  
5 voltage controlled delay elements, said differential outputs of  
6 said voltage controlled delay elements forming said plural outputs  
7 of said voltage controlled oscillator.